4. (Twice amended) The method of claim 1 [2], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

7. (Twice amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

10. (Twice amended) The method of claim 7[8], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

14. (Twice amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

17. (Twice amended) The method of claim 14[15], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

21. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein

forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

24. (Twice amended) The method of claim 21[22], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

27. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein

forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

28. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein

forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

31. (Twice amended) The method of claim 28[29], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

35. (Twice amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of bitlines coupled to the first source/drain region of the number of transistors.

38. (Twice amended) The method of claim 35[36], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

41. (Twice amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of bitlines coupled to the first source/drain region of the number of transistors.

42. (Twice amended) A method of making an information handling system, comprising:

providing a processor chip;

forming a semiconductor memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors;

forming a number of bitlines coupled to the first source/drain region of the number of transistors; and

coupling the processor chip to the semiconductor memory device with a system bus.

45. (Twice amended) The method of claim 42[43], wherein coupling a barrier [silicon nitride (SiN)] layer to the gate dielectric layer comprises composite oxidation processing to form a barrier [silicon nitride (SiN)] layer.

54. (Twice amended) A transistor formed by the following process:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, [after all source/drain regions have been formed,] wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 21, 2002, and the references cited therewith.

Claims 1, 4, 7, 10, 14, 17, 21, 24, 27, 28, 31, 35, 38, 41, 42, 45, and 54 are amended, no claims are canceled, and no claims are added; as a result, claims 1-48, and 54 are now pending in this application.

§112 Rejection of the Claims

Claims 4, 10, 17, 24, 31, 38, and 45 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.